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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/599,141	06/22/2000	Bin Yu	39153/256 (FO113)	7361

7590

05/02/2002

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EXAMINER

ROMAN, ANGEL

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 05/02/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/599,141

Applicant(s)

YU, BIN

Examiner

Angel Roman

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 1/23/02.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24, 27 and 28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24, 27 and 28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 June 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Objections

1. Claims 8 and 9 are objected to because of the following informalities: "layer" should be replaced with --material--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-3 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Chin et al. U.S. Patent 6,350,311.

Chin et al. discloses a method of manufacturing an integrated circuit, comprising; providing an amorphous semiconductor material 120 including germanium (see column

4, lines 36-39) above a bulk substrate of single crystal semiconductor material 100; annealing the amorphous semiconductor material (see column 4, lines 51-55) to form a single crystalline semiconductor layer 130 containing germanium; and doping the single crystalline semiconductor layer and the substrate at a source location and a drain location (see column 5, lines 1-5) to form a source region 160 and a drain region 160, whereby a channel region between the source region and the drain region includes a thin semiconductor germanium region (see figure 1E). Chin et al. also discloses providing a cap layer 140 before the doping step. A gate structure 150 is provided after the cap layer 140.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ouyang et al. U.S. Patent 6,319,799 in view of Chaudhari et al. U.S. Patent 4,046,618.

Ouyang et al. discloses a process of forming a transistor with a silicon germanium channel region, the process comprising; depositing a thin silicon germanium material above a top surface of a semiconductor substrate forming a single crystalline silicon germanium material 30; depositing a thin silicon material above the single crystalline silicon germanium material forming a single crystalline silicon material 34;

and providing a source region and a drain region for the transistor, the source region and the drain region extending into the substrate (see figure 2B); providing an oxide layer 18 above the silicon material 34. Ouyang et al. also discloses forming silicide layers on the source and drain regions (see column 2, lines 29-35).

Ouyang et al. is applied as above but lacks anticipation on forming the single crystalline layers by forming an amorphous material and annealing the amorphous material at a temperature between 1100-1400 degrees Celsius using an excimer laser with a 308 nanometers wavelength to form a single crystal layer; and disclosing the thickness of the layers.

Chaudhari et al. discloses forming an amorphous layer on a silicon substrate and recrystallizing the amorphous layer by annealing to form a single crystalline layer. In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to form the single crystalline layers in the primary reference of Ouyang et al. by forming an amorphous layer and recrystallizing the amorphous layer to form a single crystalline layer as disclosed in Chaudhari et al. since this is a conventional process used to form single crystalline layers. Furthermore, optimizing the process disclosed by Ouyang et al. by using a well-known method of forming a single crystalline layer is not considered to be patentable subject matter and is well within the level of a person having ordinary skills in the art.

With respect to using an excimer laser annealing at a temperature between 1100-1400 degrees Celsius with a 308 nanometers wavelength, excimer laser annealing is a conventional method used in the art for annealing semiconductor

materials (see Hamada column 6, lines 53-58) therefore it would have been obvious to one having ordinary skills in the art at the time the invention was made to use an excimer laser annealing at a temperature between 1100-1400 degrees Celsius with a 308 nanometers wavelength to perform the annealing process in the primary reference of Ouyang et al. as modified by Chaudhari et al..

Regarding the thickness for the single crystalline layers, these are conventional and obvious parameters that a person having ordinary skills in the art at the time the invention was made would have been able to determine during routine optimization of the invention disclosed by Ouyang et al..

Response to Arguments

6. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Ouyang et al., Shimbo, Kubo et al., Yamazaki, Banerjee, Vander Sande et al., Yoder et al., Schuppen et al. and Kawanaka et al. disclose semiconductor devices with channel regions including germanium.

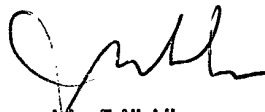
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8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

AR
April 19, 2002


John F. Niebling
Supervisory Patent Examiner
Technology Center 2800